Single-Event Upset Test Results for the Xilinx XQ1701L PROM†

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Abstract

A 3.3V serial PROM, used to configure advanced Xilinx FPGAs, was tested for single event effects with heavy ions. Device latchup was observed with an LET threshold of 55 MeV per mg/cm^2 and a saturated cross-section of 10^{-5} cm^2. Three types of upsets were measured: (1) address errors, (2) premature end-of-program signals, and (3) functional interrupt.

I. Introduction

Programmable logic devices are frequently used in space applications because of the ease of reconfiguration which significantly lowers overall cost. Earlier work has been done to investigate the effects of radiation on some of these technologies [1-6], most of which use antifuse technology for programming. The SRAM-configurable Xilinx gate-arrays require an initial programming sequence on power-up in order to setup the SRAM contents. This paper presents test results for a 3.3-V 1Mbit serial PROM that is designed to interface with Xilinx FPGAs (field programmable gate arrays) and provide the initialization sequence. This device, the XQ1701L, has a storage capacity of 1048576 bits and is currently fabricated on a bulk substrate. It can be operated in a low-current standby mode as well as in a normal mode.

The XQ1701L is a one-time-programmable read-only memory with a serial output. It is compatible with the configuration requirements of a number of 3.3-V Xilinx XC4000 and 2.5-V Virtex FPGAs which are attractive to spacecraft designers. Unsurprisingly, the configuration memory that is loaded by the PROM is SEU susceptible [3,4]. The threshold LET was approximately 5 MeV-cm^2/mg for the tested 5-V [3] and 3.3-V [4] FPGAs.

Xilinx is marketing a number of their FPGAs with a 7 μm epitaxial layer as high reliability, radiation tolerant devices in ceramic packages [7]. The "radiation tolerant" claim is based on (1) no observed SEL, (2) moderate TID levels, (3) an acceptable SEU rate, and (4) the capability of continuously monitoring the configuration SRAM for upsets. Because re-loading the FPGA takes a large fraction of a second, designs for collecting critical data or controlling expendables require a significant risk mitigation effort. These FPGAs do appear suited to a broad range of other applications, such as sensor and camera controllers.

The PROM is critical for these applications, because any errors in the PROM will cause erroneous configuration of the FPGAs with which it interfaces. The present work is the first heavy ion testing reported for these devices. Unlike the radiation-tolerant FPGAs, the configuration PROM is not fabricated on an epitaxial substrate; unsurprisingly, the PROM is susceptible to single-event latchup (SEL). The continuous monitoring capability proposed by Xilinx requires checking the SRAM contents against a known good copy, presumably from the PROM. Thus, the various PROM upset phenomena observed will cause malfunctions of configuration monitoring, making spacecraft usage more problematic.

II. Test Device Properties

Three XQ1701LCC44 (date code 9849) samples in 44-pin VQFP packages were tested, one unprogrammed (s/n: 3848) and two programmed (s/n: 3849 and 3850). Only three pins are used to exercise the devices with a fourth for the serial output and a fifth for output control. Additionally, there are three power pins; the remaining 36 pins have no connection.

The devices were programmed using a Xilinx HW130 programmer. Device 3848 was not recognized by the programmer, necessitating leaving it unprogrammed. A short section of S/N 3849 would not program to the intended pattern. The low programming success rate (one in three) may be related to the programmer itself which was not calibrated immediately prior to this use. These problems apparently did not affect the quality of the SEE data collected. The upset data collected on the two programmed devices is consistent and latchup data is consistent over all three.

The pattern programmed into the devices was approximately half "ones" and half "zeros"and was designed to permit trapping of selected types of errors. Although this does not correspond to a typical configuration pattern, it provides visibility of selected types of errors during dynamic testing.

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III. Approach Used for Radiation Testing

Heavy ions were provided by Brookhaven National Laboratory's Tandem Van de Graff accelerator. Properties of the ions used are listed in Table 1 below. Because this device has a bulk substrate, ion range is an important consideration, and is included in the table.

Table 1. Ions Used for SEU Testing

Ion	Energy (MeV)	LET (MeV-cm^2/mg)	Range (μm)
F^{19}	150	3.2	>100
Cl^{35}	210	11.5	81
Ni^{58}	260	27	40
Br^{79}	290	37	36
I^{127}	350	60	31

Dynamic testing was done on these devices during the time that they were exposed to heavy ions. A custom PCI interface card was used, connected to the device under test with a five TTL-differential line driver/receiver pairs that could drive fast signals over ribbon cable. Custom I/O routines, written in Visual C^{++} were compiled into a dynamic link library called by a user interface and DUT exerciser program in Visual BASIC running under Windows 95 on a standard personal computer.

The test apparatus is shown schematically in Figure 1. This is JPL's current generic SEE test which only requires changes in the higher level software and the test fixture to adapt to a different device.

Two different algorithms were used to determine whether the PROM functioned properly. The first algorithm began by resetting the part, and then applying a sequence of clock signals. With this algorithm, no attempt was made to compare the output of the memory. Error detection was based on detection of the end-of-address space output (CEO pin), ensuring that it only provided an output at the end of the proper number of clock cycles. If the CEO output occurred prematurely or failed to occur when expected, that indicated an error had occurred in the address control logic. The advantage of this algorithm was ease of execution. It was primarily used in initial evaluations of the device to determine what types of errors and malfunctions occurred.

The more sophisticated algorithm was used to accomplish a more complete test of the parts, executing a bit-by-bit comparison of the actual output from the PROM to the pattern it was programmed with. In particular, the pattern was chosen so that the current address being read was coded into the data. This was accomplished by creating a "marker" that the address was encoded into partitioning the device into identifiable 32 bit sections; each holding the marker and its own

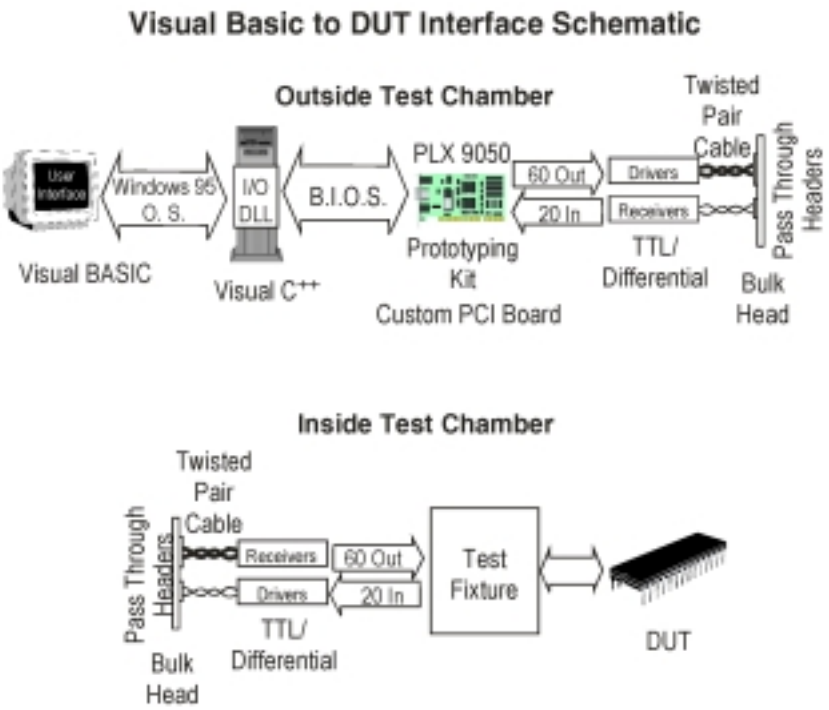

Figure 1. Schematic of the test setup.

address. Upon reading 32 bits, the test algorithm attempts to find the marker, if it does, it compares the address embedded with the last known location. Provided there is a large enough difference (in number of bits) between the last read location and the current location, the software is updated to show the address error.

There is a necessary dependence of error visibility on error rate; if errors come too fast, there are more misidentifications which tend to undercount actual errors. Getting out of synchronization with the serial data stream also means it is possible to see more bits apparently in error than actually are. With the coding scheme used, the rate of address errors seen was about 95% to 105% of those that actually occurred. Figure 2 shows results from simulations with known address error rates, assuming an equal probability that a stored logical 1 in the PROM's address storage will change to logical 0 and vice versa. The rate of observed address errors while testing varied quite a bit as the ion bombardment rate (flux) and cross sections varied, but was generally 0.003% per bit which falls very close to the 100% mark in Figure 2.

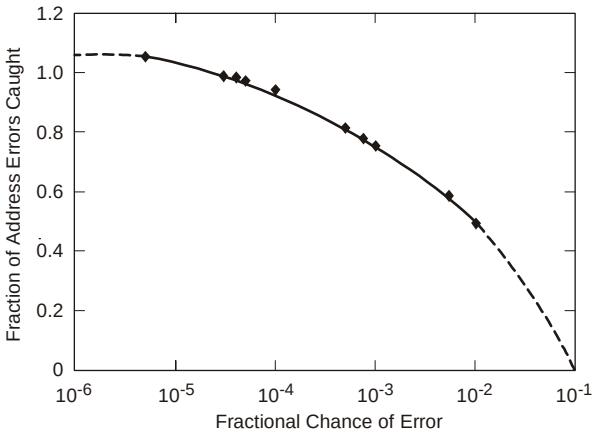

Figure 2. Simulation results of detecting address upsets.

IV. Functional Test Results

No changes in the internal stored data were observed in this PROM device. However, errors were observed in the bit stream as well as overall functionality errors. The functionality errors interfered with the quantification of bit-stream upsets: therefore, bit error cross sections were not measured.

This first type of functional error occurred in the end-of-pass output signal (EOP). That signal is of critical importance in applications of the XQ1701 device and could be detected by both of the test algorithms. The false EOP condition causes the output of the device to "freeze" and any errors that produce an erroneous EOP result will be difficult to recover from in most applications. This is the only indication of the internal address of the PROM under normal operating circumstances.

The "failed EOP" signal is seen in both algorithms but there is a difference between the two. If the EOP line erroneously goes high before 2^{20} clock strobes in the first algorithm it is counted as a failed EOP. With the second algorithm it is only considered a failed EOP if the "expected" address was not the end of the part. Hence if the EOP line is asserted before 2^{20} clock cycles, it may not be counted as an error if a suspected upset moved the internal address to the end of the device.

During SEU tests, a number of EOP errors

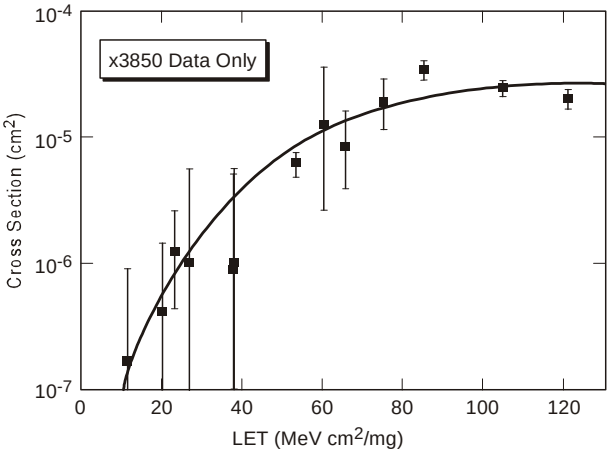

Figure 3. Cross section for end-of-pass errors in the Xilinx XQ1701L PROM. (curve after ref. 8)

occurred. Figure 3 shows how the cross section for EOP errors depends on LET. The threshold LET is approximately 8 MeV-cm^2/mg where the definition of threshold for this device is the LET where the cross section drops below $10^{-7}cm^2$ (i.e. experimentally observable). The cross section gradually increases by about two orders of magnitude with increasing LET. EOP errors persist until the part undergoes reset or power cycling. Note the curve shown in Fig. 3 is fitted to the physically based model of Ref. 8.

Address failures were also observed during the SEU tests. The address failures were observed by comparing the actual location of data within the device with the expected location based on the number of data strobe cycles. Though the actual address errors were not recorded as to before and after location, it is expected that address errors could go forward and backward in the part, and that jumps would correspond to upsetting an address register somewhere. Thus errors were expected to be relocations of the output stream by 2^x bits where x can range from zero to nineteen. Figure 4 shows how the cross section for address errors depends on LET. The threshold LET was approximately 8 MeV-cm^2/mg based on a model discussed later. Recovery from address failures

required reset or power cycling.

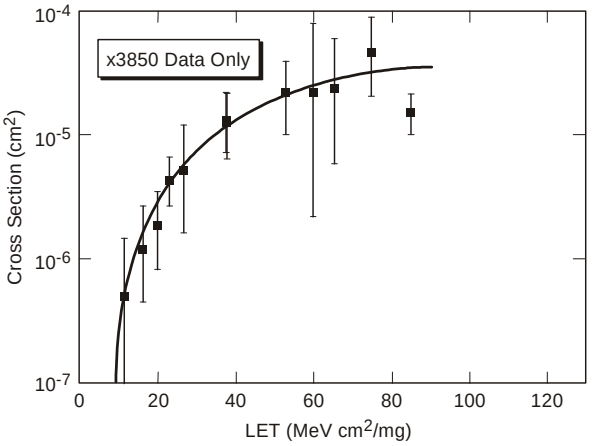

Figure 4. Cross section for address errors in the Xilinx XQ1701L PROM. (curve after ref. 8)

Several events were also observed where part functionality was lost, and the operating current decreased to very low values, implying that the device had been triggered into a standby-like operating mode. However, the only way to recover from this mode was to initiate power cycling, which is not required to recover from normal standby. As shown in Figure 5, the cross section for these functional interrupt (SEFI) errors is similar to that of the other two types of functional errors. It is likely that a common design is used to implement their storage elements, and the number of elements involved in the three upset modes is similar (within a factor of 8 or so). Also of note in Figure 5 is the lack of data between LET 23 and LET 55 which is due to no observed events. The fluence on these runs was small and they show the subtle difference in cross section between the SEFI error and the other error discussed here.

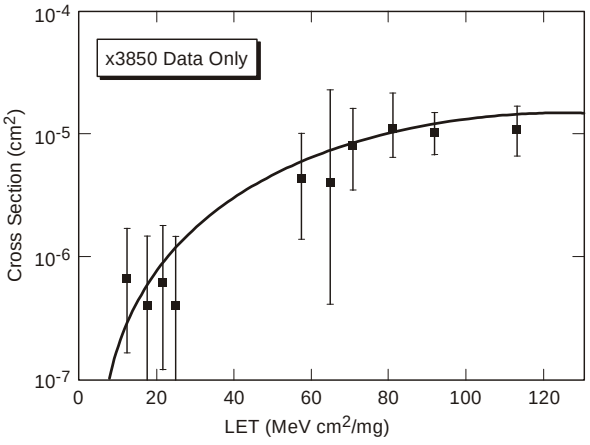

Figure 5. Cross section for SEFI events which resulted in loss of output functionality accompanied by low operating currents. (curve after ref. 8)

Table 2 summarizes the three types of functional errors that occurred, along with the required sequence to recover from the erroneous condition. The devices always recovered completely provided the proper recovery method was used. None of the errors affected the programmed bits of the PROM.

Table 2. Functional Errors Observed
During SEU Tests of the XQ1701L PROM

Error Type	Circuit Effect	Recovery Method
EOP	False EOP signal; output lockout	Reset or power cycle
Address	Address error	Reset or power cycle
SEFI	Stuck output low operating current	Power cycle required

During testing, SEFI occurred in many instances where data on false EOP and address errors occurred. Though power cycling would work, continued irradiation of parts undergoing SEFI was usually adequate to bring parts back to operation. Thus, the cross section for exit from SEFI is approximately equal to the enter SEFI cross section. It seems likely that a single symmetrical flip-flop is involved. Data collected during runs with multiple SEFIs requires a correction for dead time in every reading because no other failure modes were observable while in the low current state. The dead time during SEFI can be seen in Figure 6 as the section of the strip chart where the current falls to 0. Note that it is approximately half the run.

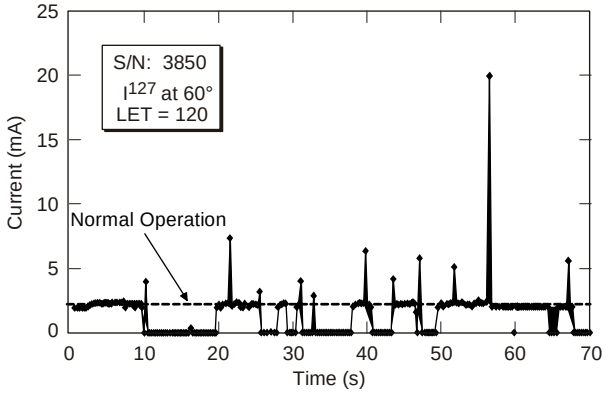

Figure 6. The current strip chart of a typical run (5.1×10^5 ions of I^{127} in 65s) in which a single latchup occurred and 7 SEFIs.

V. Statistical Observations

Because of the desire to catch several types of possible errors simultaneously, flux rates were kept at low level except in a few SEL runs. The actual number of events per run was small, requiring a small value approximation for the statistical error in a Poisson random variable. Some runs with no detected errors have been left out of the figures for clarity, provided the error bars would allow them to remain on the trend. Also of statistical note is the interplay between the error modes discussed. As mentioned earlier, the flux was turned down as far as reasonable in order to keep individual error types distinct. Nevertheless there is an interplay between the four error types; the data presented are corrected for this interplay as much as possible. Runs with latchup did not show latchup to significantly impact the other error types, except that the part had to be reset upon latchup. The SEFI mode did cause major difficulties for some of the runs and accounted for up to half the fluence in some cases. The other interplay came from address errors that were not properly identified before the part correctly asserted the EOP signal. Computer simulation of device behavior shows that this only contributes about one wrong false EOP event per 1000 address fails, and since none of the data even came near 1000 address fails, this interplay is safely ignored.

VI. Latchup Test Results

Latchup test results are shown in Figure 7. Iodine was the only ion used that showed SEL at normal incidence. Other than its LET of 59.8, all other data points are with ions at angle. These other points follow the sort of trend expected, with Iodine's 59.8 falling in place. This implies that the cosine law is reasonable for this device over the range of angles used, even though this is a bulk

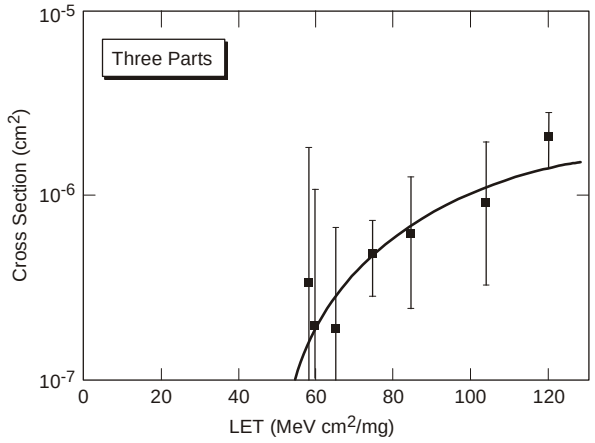

Figure 7. Cross section for latchup in the XQ1701L PROM. (curve after ref. 8)

device and the effective ranges of the ions that caused latchup are from 18 to 30μm.

No latchup was detected for LET=53 to a fluence of $4.1 \times 10^7/cm^2$. Thus, the threshold LET for latchup is approximately 55 MeV-cm^2/mg. Latchup results for the unprogrammed device (x3848) under static bias were consistent with dynamic results obtained for the other two samples.

During latchup testing, the higher than normal operating current was detected and measured within about 100 ms. After 500 ms, power was temporarily removed. Latchup equilibrium voltages – that is, the voltage reached by the device during latchup with the current limited to 20 mA – were measured for each latchup event. A histogram of these voltages is shown in Figure 8. The voltage distribution for the majority of latch-ups ranges from 2 to 3V centering around 2.4 V which corresponds to a 120Ω current path through the part. It appears there are only two types of

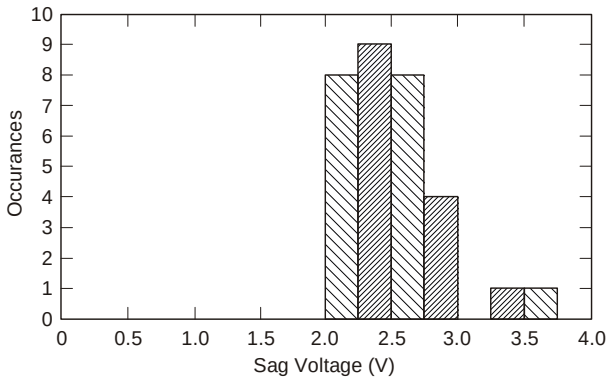

Figure 8. Histogram of equilibrium voltages that occurred just after latchup in the XQ1701L PROM

structures on the device subject to SEL.

VII. Discussion

Four different SEE modes were observed during SEU tests of the XQ1701L PROM device. These included three functional operational modes: (1) end-of-program errors; (2) address errors; and (3) SEFIs. The first two types of errors could be recovered from by applying a reset signal to the device, but the third type of error could only be recovered from by cycling the power.

All three types of functional errors had similar threshold LET values and cross sections. The data were fit with a two-parameter fitting function [8], which has a physical basis and fits many data sets better than the four-parameter Weibull function. Preference was given to the data points taken at normal incidence when selecting the fitting parameters, because other data points can be

influenced by range limitations. Data and fits are shown in Figures 3-5 and 7.

Event rates are calculated by combining a cross section curve with environmental data via the IRPP method [9]. Ion range limitations prohibit meaningful measurements of the angular dependence of the directional cross section at very large angles, so the ratio of RPP thickness to lateral dimensions that will correctly predict the angular dependence seen by high-energy particles is uncertain. Motivated by past experience (e.g., comparisons between rate predictions and flight observations), the RPP thickness was selected to be one-fifth of the lateral dimensions.

Using a standard galactic cosmic ray (GCR) model, the probability of a functional error (not SEL) during solar maximum GCR is estimated to be 0.19% per device-year of operation. Calculations were also done using the solar flare heavy ion model (at 1 AU and behind 100 mil aluminum shield) developed by JPL. The probability of a functional error from such a flare, given that one such flare occurs, is calculated to be 1.0%. Similar calculations for SEL estimate probabilities that are 1000 times smaller than that for functional failures.

However, those error rates do not consider the possibility of upset from protons. Proton testing was not done, but other devices on bulk substrates have been sensitive to proton upset when the LET threshold was below approximately 8 MeV-cm^2/mg.

The PROM is also susceptible to latchup, but only at relatively high LET (40 MeV-cm^2/mg). Because of the high threshold LET, the probability of latchup is relatively low in these devices, and the risk is probably acceptable for most applications.

One way to mitigate SEU effects in these devices is to control the time period during which they operate. Since they are only used to initialize FPGA devices during start-up periods, it is relatively straightforward to minimize the time which they are powered. An alternative approach is to cycle the power in the PROM just before configuring or reconfiguring the FPGA devices that are driven by the PROM to avoid the functionality errors that can be induced by SEU effects. How-ever, this is less desirable because latchup, if it occurs, would continue for extensive periods until the next power cycle occurs. Either approach precludes continuous comparison of the FPGA configuration with the PROM.

SEE effects in the XQ1701L do not preclude its use in space, but designers must choose between assuming the small risk of mission failure or assuring that the functional errors caused by heavy ions do not cause catastrophic system effects. Although proton testing was not done, the low threshold LET makes it likely that protons will cause all three upset phenomena in the PROM to occur. This will increase the estimated error rates, particularly in earth-orbiting systems that have to pass through the earth's proton belts, and systems that endure flares. To reduce (or eliminate) in flight SEL risk users may wish to wait for Xilinx to release the 7μm epi replacement PROM currently under development and expected to have better latchup performance [7].

VIII. REFERNCES

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